

**APPLICATION FOR LETTERS PATENT
OF THE UNITED STATES**

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TITLE OF INVENTION: CONTROLLED SUBSTRATE VOLTAGE FOR
MEMORY SWITCHES

TO WHOM IT MAY CONCERN, THE FOLLOWING IS
A SPECIFICATION OF THE AFORESAID INVENTION

CONTROLLED SUBSTRATE VOLTAGE FOR MEMORY SWITCHES

FIELD OF THE INVENTION

The invention relates generally to semiconductor memory integrated circuits (“ICs”), such as dynamic random access memories (“DRAMs”), and, more particularly, to a controlled substrate voltage for such ICs.

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BACKGROUND OF THE INVENTION

Dynamic random access memories (“DRAMs”) are the most commonly manufactured product of all semiconductor integrated circuits (“ICs”). DRAMs are data storage devices that store data as a charge on a storage capacitor. A DRAM typically includes an array of memory cells. Each memory cell includes a storage capacitor and a transistor for transferring charges to and from the storage capacitor. Each memory cell is addressed by a word line (“WL”) and accessed by a bit line (“BL”) pair. The WL controls the transistor such that the transistor couples the storage capacitor to and decouples the storage capacitor from the BL pair for writing data to and reading data from the memory cell. Multiple word lines correspond to multiple rows of memory cells, while multiple bit line pairs correspond to multiple columns of memory cells.

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DRAM array devices should be designed with minimum leakage currents so as to be capable of supporting as high as possible retention times. Therefore, the substrate voltage is conventionally connected to negative voltage levels, such as -0.5 V, to reduce leakage

currents. However, this can result in increased source to substrate voltages, thereby increasing the threshold voltage and reducing device performance (e.g., reduced write back current). Additionally, DRAM devices may not share a common substrate, but may have individual substrate wells. Examples of such DRAM devices include silicon on insulator (“SOI”) DRAMs and vertical (e.g., trench technology) DRAM devices with complete body pinch off due to the buried strap (“BS”) beyond the cell dimensions. The BS provides the outdiffusion from the trench to the drain of the array device, thereby providing connection. Since the BS diffuses horizontally, it can eventually connect to the next trench, isolating the well.

It is therefore desirable to provide a solution that can reduce the increase in the array device threshold voltage. Exemplary embodiments of the invention actively adjust the substrate well voltage during operation of the memory device. This can reduce the body effect (i.e., variation of the threshold voltage due to a variation of the substrate or bulk voltage) and can therefore provide improved array device performance (e.g., reduced data corruption) while the word line (“WL”) is activated.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and further advantages of the invention may be better understood by referring to the following description in conjunction with the accompanying drawings in which corresponding numerals in the different figures refer to the corresponding parts, in
5 which:

FIGURE 1 diagrammatically illustrates a DRAM circuit implementation in accordance with the known art;

FIGURE 2 diagrammatically illustrates exemplary embodiments of a DRAM circuit implementation in accordance with the present invention;

10 FIGURE 3 diagrammatically illustrates a vertical cell layout in accordance with the known art; and

FIGURE 4 diagrammatically illustrates exemplary embodiments of a vertical cell layout including body contacts in accordance with the present invention.

DETAILED DESCRIPTION

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While the making and using of various embodiments of the present invention are discussed herein in terms of specific sensing schemes and voltage conditions, it should be appreciated that the present invention provides many inventive concepts that can be embodied in a wide variety of contexts. The specific embodiments discussed herein are merely illustrative of specific ways to make and use the invention, and are not meant to limit the scope of the invention.

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The present invention provides a solution that can reduce the increase in the threshold voltage of dynamic random access memory (“DRAM”) devices, thereby improving device performance during operation. The use of body contacts as described herein can provide variable substrate voltages during DRAM operation. The body contacts can change the body bias of activated memory cells, while maintaining the body bias of inactive memory cells. This can reduce the body effect (i.e., variation of the threshold voltage due to a variation of the substrate or bulk voltage) and can therefore provide improved array device performance (e.g., reduced data corruption) while the word line (“WL”) is activated.

FIGURE 1 diagrammatically illustrates a DRAM circuit implementation 100 in accordance with the known art. Word line driver final stage 110 drives WL 120 which is connected to memory cells 130 and 140. Values are read out of memory cells 130 and 140 on bitlines (“BL”) 137 and 147, respectively. Memory cells 130 and 140 include transistor

switches 133 and 143, respectively. Substrate wells 135 and 145 of transistors 133 and 143, respectively, are each connected to a fixed potential of -0.5 volts.

Exemplary embodiments of the present invention can modify circuit implementation 100 to include transistor 210, body contact 220, and resistor 230, as illustrated in FIGURE 2.

5 Source 213 and gate 215 of transistor 210 can be connected to final stage 110 and WL 120, respectively. Drain 217 of transistor 210 can connect to resistor 230 through body contact 220. Transistor 210 is coupled to body contact 220 which is connected to substrate wells

10 135 and 145 of memory cells 130 and 140. In some exemplary embodiments, a body contact, such as 220, can be connected to the substrate wells of all array devices connected to

15 a word line, such as WL 120. In the exemplary embodiment illustrated in FIGURE 2, if WL 120 is inactive, body contact 220 will be connected to a fixed potential of -0.5 volts via resistor 230. Once WL 120 is activated, the potential at body contact 220 will be adjusted to 0 volts as long as the on-resistance of transistor switch 210 is considerably lower (e.g., 5-10x

lower) than the resistance of resistor 230. This can result in reduced body effect and improved array device performance while WL 120 is activated.

FIGURE 3 diagrammatically illustrates a vertical cell layout 300 in accordance with the known art. Trench memory cells 310 each have a single buried strap (shown in black). Cells 310 are addressed by their respective WL 320 and have respective non-isolated (i.e., connected to a wafer substrate) substrate wells 330.

Exemplary embodiments of the present invention can provide body contact rows 410, as illustrated by the exemplary vertical cell layout 400 of FIGURE 4. Each body contact row 410 can, in some embodiments, correspond to a respective body contact 220 (see also FIGURE 2), thereby to ensure a defined voltage level at substrate wells 430 as described above.

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Although exemplary embodiments of the present invention have been described in detail, it will be understood by workers in the art that various modifications can be made therein without departing from the spirit and scope of the invention as set forth in the appended claims.

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